

Multicore Computer Architecture - Storage and Interconnects

Tutorial 1A

Instruction Pipeline & Performance



NPTEL Online Course : Multi-Core Computer Architecture and Interconnects Dr. John Jose, IIT Guwahati

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Tutorial Problem-1

- ❖ Consider a code fragment $A = D * (B + C) - E$ (where A, B, C, D and E are memory locations) to be executed on a processor TITAN. Write down the instruction sequence generated for this code fragment if TITAN is (a) Stack machine (b) Accumulator machine (c) Load Store machine.

Tutorial Problem-1

❖ $A = D * (B + C) - E$

Accumulator machine

Load Store machine

Stack machine

❖ Push D

❖ Push B

❖ Push C

❖ Add

❖ Mul

❖ Push E

❖ Sub

❖ Pop A

❖ Load B

❖ Add C

❖ Mul D

❖ Sub E

❖ Store A

❖ Load R1, D

❖ Load R2, B

❖ Load R3, C

❖ Add R4, R2, R3

❖ Mul R5, R1, R4

❖ Load R6, E

❖ Sub R7, R5, R6

❖ Store R7, A

Tutorial Problem-2

- ❖ The time delay of a 4-segment pipeline in different segments are $t_1=35$ ns, $t_2 = 30$ ns, $t_3 = 40$ ns, $t_4=45$ ns. The interface register delay time is $t=5$ ns. How long would it take to complete 100 instructions in the pipeline ? (Assume there is no dependency between the instructions).

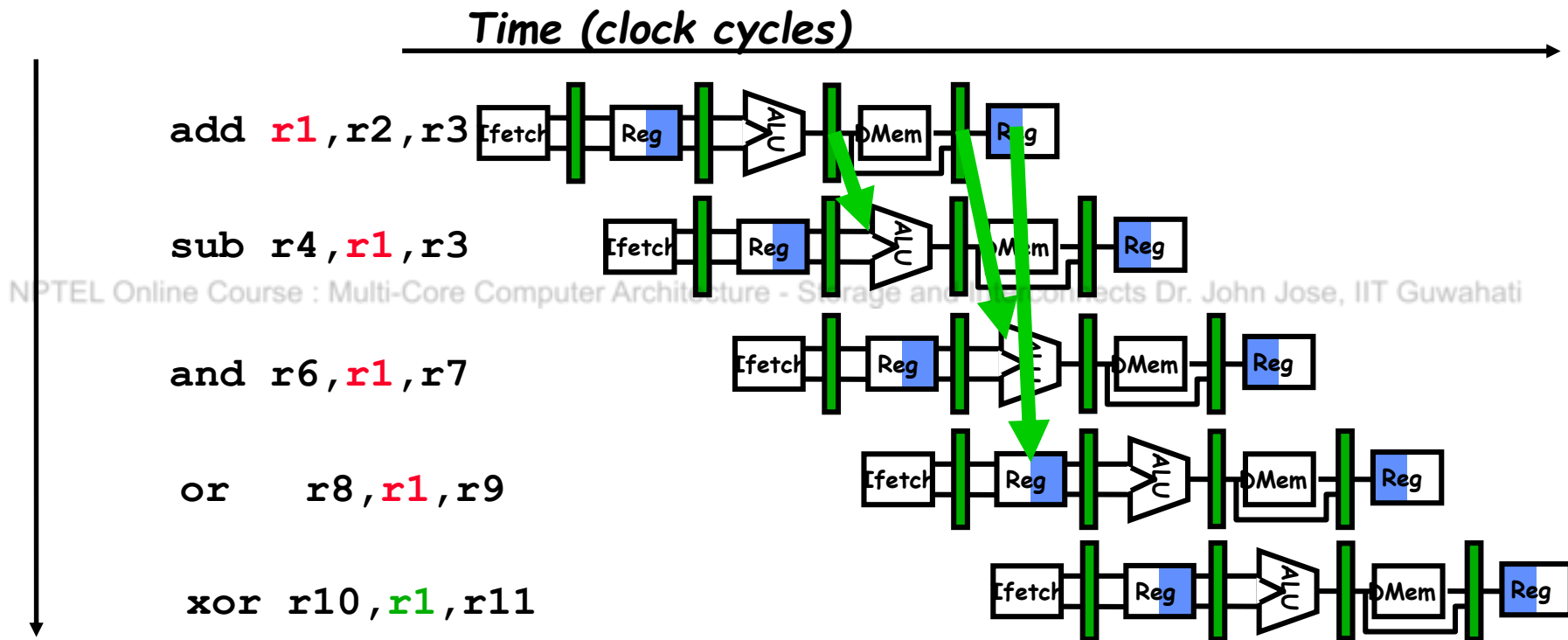
Tutorial Problem-3

❖ Which of the following statements is/are TRUE?

- (I) RAW data hazard could be reduced by operand forwarding.
- (II) A normal in-order 5 stage MIPS pipeline can achieve an IPC larger than 1.
- (III) For a MIPS instruction `STR R2, 16(R3)`, some contents stored in its ID/EX pipeline register will bypass the EX unit directly to EX/MEM pipeline register.
- (IV) A normal 5 stage in order RISC pipeline without operand forwarding can have RAW and WAR hazards.

(A) I only (B) I & III only (C) II & IV only (D) III & IV only

Operand Forwarding to Avoid Data Hazard



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Visualizing Pipelining

Instruction number	Clock number							
	1	2	3	4	5	6	7	8
i	IF	ID	EX	MEM	WB			
$i+1$		IF	ID	EX	MEM	WB		
$i+2$			IF	ID	EX	MEM	WB	
$i+3$				IF	ID	EX	MEM	WB
$i+4$					IF	ID	EX	MEM

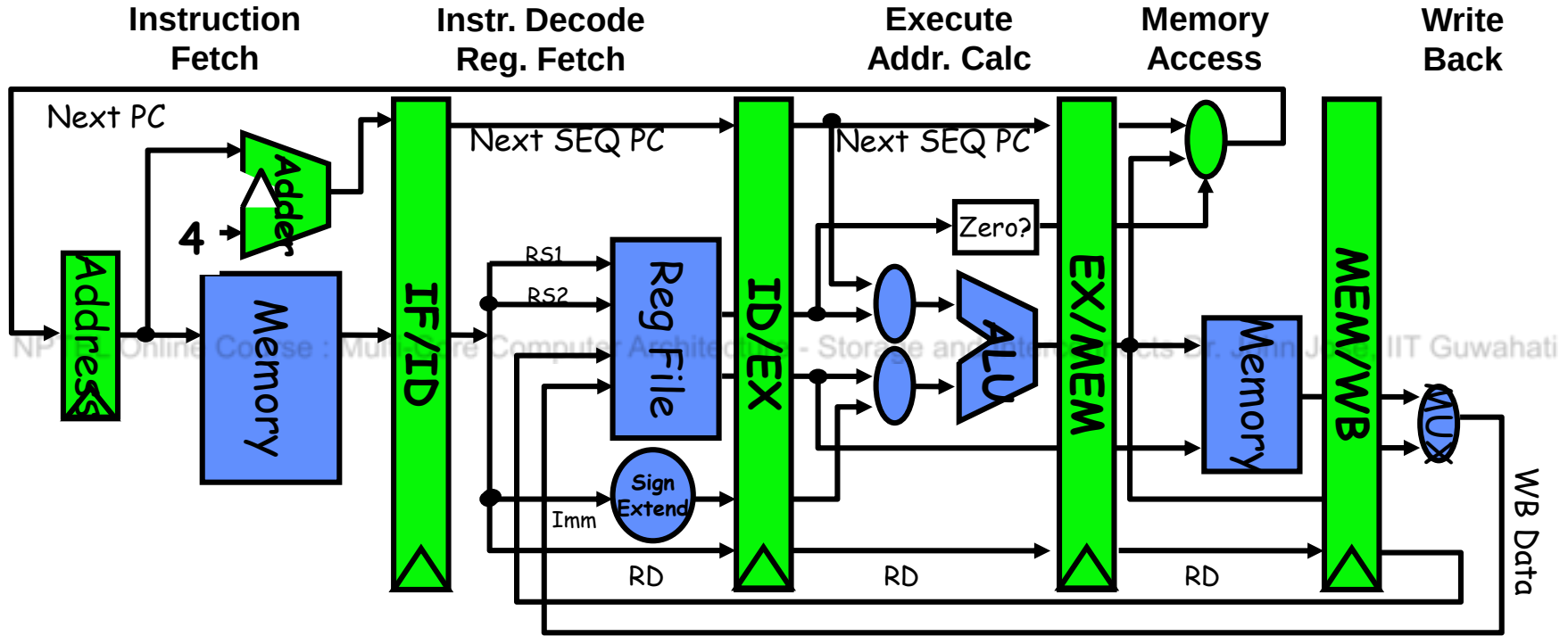
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Pipelined RISC Data path



STR R2, 16(R3)

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$i+4$					IF	ID	EX	MEM

add **r1**, r2, r3
 sub r4, **r1**, r3
 and r6, **r1**, r7

add r1, r2, **r3**
 sub **r3**, r1, **r4**
 and **r4**, r1, r7

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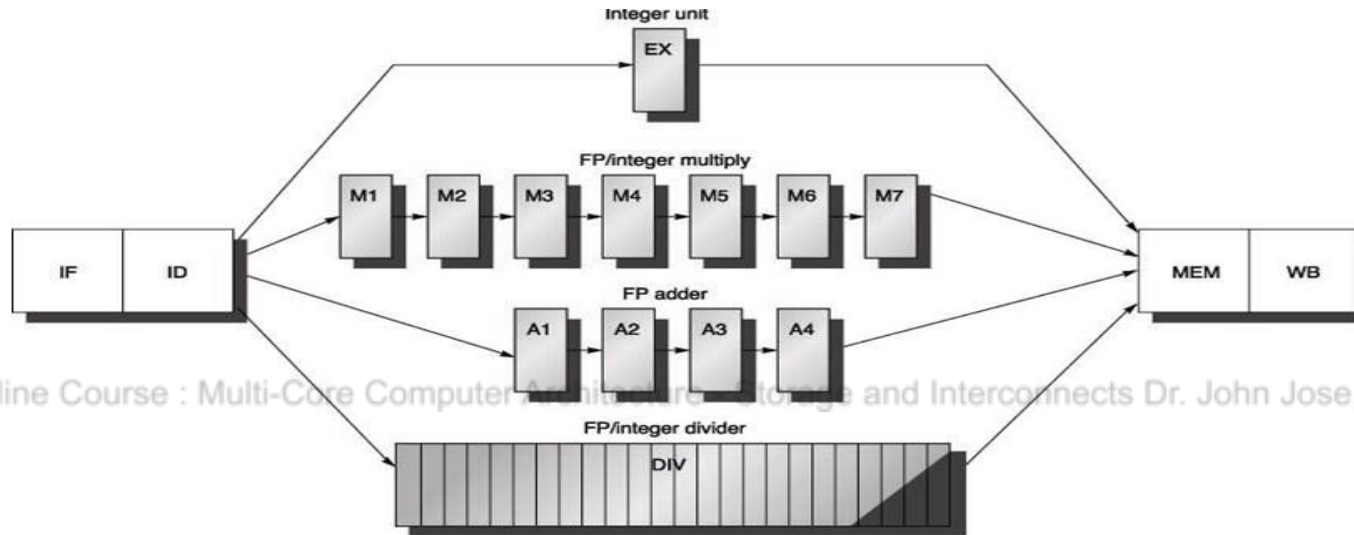
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Tutorial Problem-4

❖ Which of the following statements is/are FALSE?

- (I) For a MIPS multi-cycle floating point pipeline the initiation interval of FP-mul is larger than that of FP-add
 - (II) WAW hazard cannot happen in a MIPS multi-cycle floating point pipeline.
 - (III) In a MIPS multi-cycle floating point pipeline that supports operand forwarding, there will be 7 stalls between a pair of adjacent MUL instructions that has a RAW dependency between them.
 - (IV) If a 32 bit value (0x12345678) is stored in memory byte addresses 2000, 2001, 2002 and 2003 in big-endian format, then location 2001 holds the value 0x56.
- (A) III only (B) I only (C) I & IV only (D) I, II, III & IV

Multi-cycle Operations



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Functional unit	Latency	Initiation interval
Integer ALU	0	1
Data memory (integer and FP loads)	1	1
FP add	3	1
FP multiply (also integer multiply)	6	1
FP divide (also integer divide)	24	25

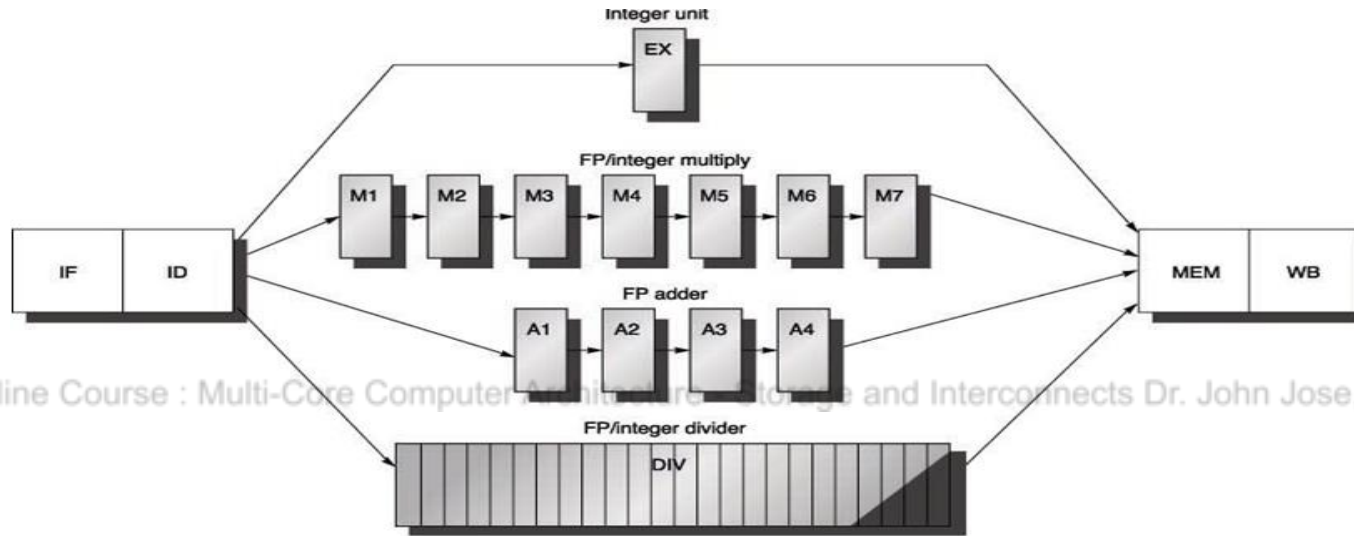
Latencies and initiation intervals for functional units.

Tutorial Problem-4

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Multi-cycle Operations



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MUL.D	IF	ID	<i>M1</i>	M2	M3	M4	M5	M6	M7	MEM	WB
ADD.D		IF	ID	<i>A1</i>	A2	A3	A4	MEM	WB		
L.D			IF	ID	<i>EX</i>	MEM	WB				
S.D				IF	ID	<i>EX</i>	MEM	WB			

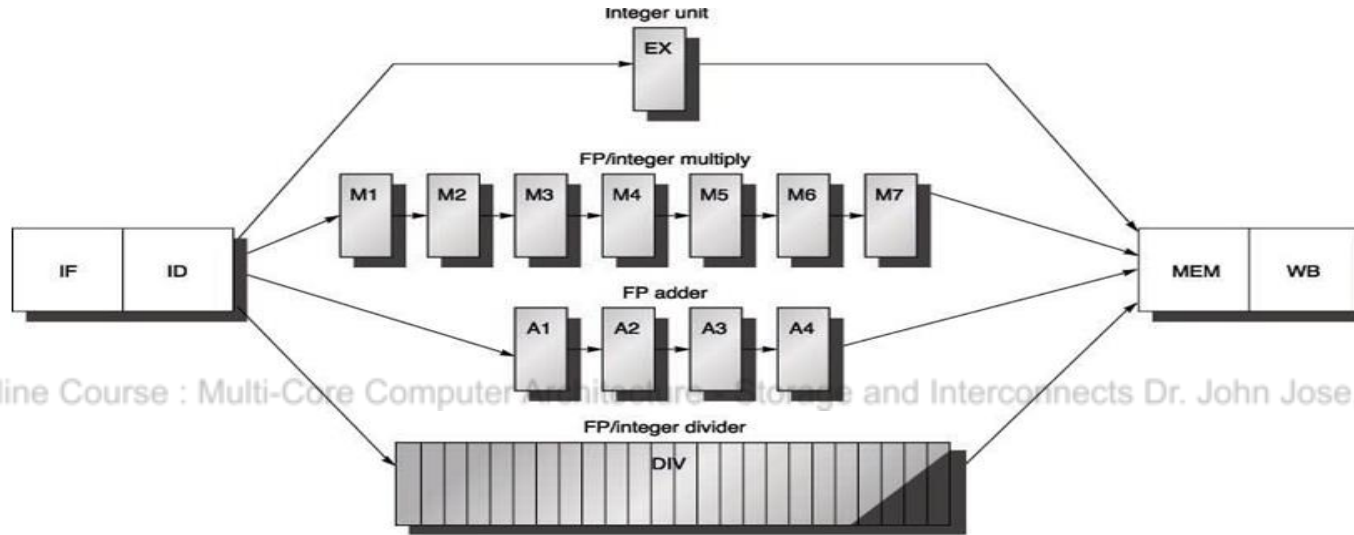
The pipeline timing of a set of independent FP operations. The stages in italics show where data are needed, while the stages in bold show where a result is available. The ".D" extension on the instruction mnemonic indicates double-precision (64-bit) floating-point operations. FP loads and stores use a 64-bit path to memory so that the pipelining timing is just like an integer load or store.

Tutorial Problem-4

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Multi-cycle Operations



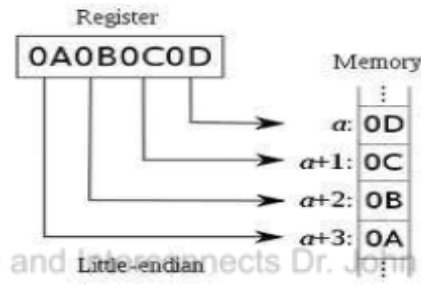
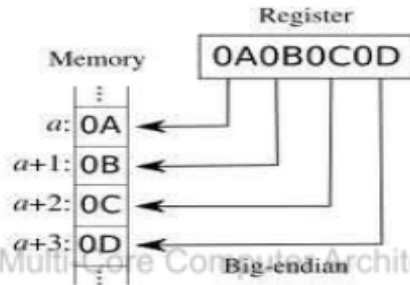
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Byte Ordering

Big Endian vs. Little Endian



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Tutorial Problem-5

- ❖ A new floating-point unit speeds up floating point operations by two times. In an application one fifth of the instructions are floating-point operations.
 - (a) What is the overall speedup? (Ignore the penalty to other instructions).
 - (b) Assume that the speeding up of the floating-point unit mentioned above slowed down data cache accesses resulting in a 1.5x slowdown. Assume the load instructions constitute 15% and store instructions constitute 9% of the total instruction what is the effective overall speedup now?

Amdahl's Law:

$$Speedup = \frac{1}{(1 - \alpha) + \frac{\alpha}{n}}$$

Tutorial Problem-5

Amdahl's Law:

$$Speedup = \frac{1}{(1 - \alpha) + \frac{\alpha}{n}}$$

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Tutorial Problem-6

- ❖ Given a non-pipelined architecture running at 1GHz, that takes 5 cycle to finish an instruction. You want to make it pipelined with 5 stages. The increase in hardware forces you to run the machine at 800MHz. The only stalls are caused by - memory - (30% of the total instructions) a stall of 70 cycles happens in 2% of the memory instructions - branch - (20% of the total instructions) a stall of 2 cycles happens in 20% of the branch instructions. What is the actual speedup obtained by pipelining?

Tutorial Problem-6

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**THANK
YOU!**

**FOR
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